REMARKS

The claims are claims 1 to 7 and 9 to 12.

The title has been amended as requested by the Examiner.

The application has been amended at several locations to correct minor errors and to present uniform language throughout. The amendments include correction of those errors noted by the Examiner.

Claims 1, 9 and 10 are amended. Claim 8 is canceled. Claim 1 has been amended to incorporate limitations previously recited in canceled claim 8. Claims 9 and 10 have been amended to depend upon claim 1.

Claims 1 to 7 and 9 were rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,297,242 to Miki. Regarding original claim 1, the OFFICE ACTION states at page 3, lines 19 to 22:

> "a source word size register storing a source word size (fig 2, element 201, element labeled "PW1", column 3 lines 53-68), and
> a target word size register storing a target word size (fig 2, element 202, element labeled "PW2", column 3, lines 53-68)"

Regarding original claim 8, the OFFICE ACTION states at page 5, lines 18 and 19:

> "a source increment size register storing a source increment size (fig 2, element 201, element labeled "BW1 ", column 3, lines 53-68)"

and the OFFICE ACTION states at page 6, lines 1 and 2:

> "a target increment size register storing a target increment size (fig 2, element 202, element labeled "BW2", column 3, lines 53-68)"

The Applicants respectfully submit that this understanding of the teaching of Miki is incorrect.

Claim 1 recites subject matter not anticipated by Miki. Claim 1 recites "a source word size register storing a source word size," "a target word size register storing a target word size," "a source increment size register storing a source increment size" and "a target increment size register storing a target increment size." The Applicants respectfully submit that Miki fails to teach independent specification of the data size and increment size for the source and target. The OFFICE ACTION cites four registers BW1, BW2, PW1 and PW2 as anticipating four registers recited in claim 1. The Applicants respectfully submit that Mike fails to teach that registers BW1 and PW1 are used at the same time as registers BW2 and PW2. Mike teaches at column 3, lines 53 to 55 that parameter registers 201 and 202 "correspond to respective DMA transfer channels." Figure 3 of Miki illustrates supply of PW1 and BW1 to both write control circuit 1007 and read control circuit 1008. Thus these four register would not be used together to control a single data transfer operation. On the contrary, Miki teaches that these four registers would be employed separately in pairs in separate DMA transfers controlled by separate DMA channels. Accordingly, claim 1 is allowable over Miki.

In addition, claim 1 Claim 1 further recites the direct memory access unit transfers data "by recalling data from a first bus data supplying device beginning at said source start address and thereafter at successive addresses differing by said source increment size in a data size corresponding to said source word data size and supplying said recalled data to a first bus data receiving device beginning at said target start address and thereafter at successive addresses differing by said target increment size in a data size corresponding to said target word

size." Thus the data size and the increment size are specified by different registers for both the source and target. Miki clearly teaches that the same registers control both address incrementing and data size selection. Miki states at column 4, lines 26 to 45:

> "MPX 1071 selects and outputs the port width PW when the data transfer direction TD is '1' to designate the data transfer from a memory to a peripheral I/O. On the other hand, when TD is '0' to designate the data transfer from a peripheral I/O to a memory, MPX 1071 selects and outputs the bus width BW. Each of the port width PW and bus width BW consists of 2 bits, with '00' being a 8-bit width, '01' being a 16-bit width and '10' being a 32-bit width. INC 1072 increments the content of WP 1073 by a value responsive to the output data from MPX 1071 and rewrites the incremented value into WP 1073. WP 1073 is of 3 bits construction. When the output of MPX 1071 is '00', the content of WP 1073 is incremented by 1, when '01', incremented by 2, and when '10', incremented by 4. The write decoder 1074 responds to the content of WP 1073 and the output data of MPX 1071 to control levels of 8 write-enable signals W10 to W23 in accordance with FIG. 4. These signals W10 to W23 are supplied to write-enable terminals WE of the registers R10 to R23, respectively."

Miki clearly discloses that the data from the register selected by multiplexer 1071 controls the increment amount of incrementer 1072 and the controls the data width by controlling the write enable terminals of write decoder 1074. Miki includes similar disclosure for the read control circuit 1008 at column 4, lines 46 to 64. Because Miki teaches the same source data for incrementing and data size, it does not anticipate the recitations of differing registers controlling data size and incrementing of claim 1. Thus claim 1 is allowable over Miki.

Claims 2 to 7 and 9 to 12 are allowable by dependence on allowable claim 1.

The Applicants respectfully submit that all the present claims are allowable for the reasons set forth above. Therefore early reconsideration and advance to issue are respectfully requested.

If the Examiner has any questions or other correspondence regarding this application, Applicants request that the Examiner contact Applicants' attorney at the below listed telephone number and address to facilitate prosecution.

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Respectfully submitted,

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